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CHIP PACKAGE AND PROCESS THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention generally relates to a chip package and a process thereof, and more particularly to a chip package having a rigid cover on the active surface of the chip and a process thereof.

Description of Related Art

[0002] In the semiconductor industry, integrated circuit (IC) manufacturing includes 3 steps – design, process, and packaging. Chips are manufactured by the steps of making wafer, designing the circuit, making the mask, sawing the wafer and so on. Each chip is electrically connected to the external circuit via the bond pads on the chip. Then the insulating material is optionally used to package the chip. The purposes of packaging are to protect the chip from moisture, heat and noise, and to provide the electrical connection between the chip and the external circuit such as printed circuit board (PCB) or other carriers.

[0003] As the IC packaging technology advances, the package is getting smaller. Among the IC packaging types, chip scale package (CSP) is one of the package technologies that the length of the package is smaller than 1.2 times of the length of the chip inside the package, or (the chip area/ package area) is smaller than 80% while the pitch of the pins of the package is smaller than 1mm. Based on the material and the structures, CSP includes rigid interposer type, flex interposer type, custom lead frame type, wafer level type and so on.

[0004] Unlike the packaging technology for single chip, the wafer level package focuses on packaging wafer in order to simplify the chip packaging process. Hence, after the integrated circuits have been manufactured on the wafer, the whole wafer can be packaged. Then the wafer sawing can be performed to form a plurality of chips from the wafer.

SUMMARY OF THE INVENTION

[0005] An object of the present invention is to provide a chip package having a better structural strength, thermal conductive efficiency, and anti-electromagnetic interference ability.

[0006] Another object of the present invention is to provide a chip packaging process using wafer level package technology in order to provide a better structural strength, thermal conductive efficiency, and anti-electromagnetic interference ability.

[0007] The present invention provides a chip package, comprising: a chip having an active surface and a plurality of bond pads, the bond pads being on the active surface; and a rigid cover on the active surface, the rigid cover exposing the bond pads above the active surface.

[0008] In a preferred embodiment, the chip includes a Re-Distribution Layer (RDL) on the active surface to form the bond pads.

[0009] In a preferred embodiment, the rigid cover is adhered to the active surface. The rigid cover can have a periphery thereof adhered to the active surface. The rigid cover includes a conducting material, an insulating material, or a transparent material.

[0010] In a preferred embodiment, the chip package further comprises a plurality

of contacts on the bond pads respectively, and the contacts' heights relative to the active surface are larger than the rigid cover's height relative to the active surface.

[0011] In a preferred embodiment, the bond pads can be disposed on the circumference of the active surface. The bond pads are disposed on the active surface as an area array, and the rigid cover has a plurality of openings to expose the bond pads respectively. When the active surface is a rectangle, the bond pads are disposed on a one outside of the rectangle. The chip has a backside relative to the active surface and a plurality of connecting lines, each connecting lines having an end connected to one of the bond pads, the connecting lines extending to the backside via a lateral side of the chip and forming a plurality of terminal pads on the backside respectively.

[0012] In a preferred embodiment, the terminal pads are disposed around the circumference of the backside of the chip. The terminal pads can also be disposed on the backside of the chip as an area array. Further, the chip package can comprise a plurality of contacts on the plurality of terminal pads respectively.

[0013] The present invention provides a chip packaging process, comprising: providing a wafer, the wafer having an active surface and a backside corresponding to the active surface, the wafer having a first chip area and a second chip area adjacent to the first chip area, the wafer having a plurality of first and second bond pads on the active surface in the first and second chip areas respectively; forming a plurality of through holes on the wafer, the plurality of through holes passing through the wafer and connecting the active surface and the backside, the through holes being arranged between the first chip area and the second chip area; forming a plurality of first and second connecting lines on the wafer, each of the plurality of first connecting lines having a first end through one of the through holes electrically connected to one of first

bond pads, each of the first connecting lines having a second end extending to the backside of the first chip area to form one first terminal pad on the backside of the first chip area, each of the second connecting lines having a first end passing through one of the through holes electrically connected to one of second bond pads, each of the second connecting lines having a second end extending to the backside of the second chip area to form one second terminal pad on the backside of the second chip area, a portion of the first connecting lines in the through holes being connected to a portion of the second connecting lines in the through holes respectively; disposing a first rigid cover and a second rigid cover on the active surface of the first chip area and the active surface of the second chip area respectively; sawing the wafer along an area between the first and second chip areas and sawing the portions of the plurality of first connecting lines in the through holes and the portions of the second connecting lines in the through holes respectively; and separating the first chip area and the second chip area from the wafer, the first chip area of the wafer and the first rigid cover being a first chip package, the second chip area of the wafer and the second rigid cover being a second chip package.

[0014] In a preferred embodiment, before the step of separating the first chip area and the second chip area from the wafer, the process further comprises forming a plurality of contacts on the first and second terminal pads. The first rigid cover can be adhered to the active surface. The first rigid cover can have a periphery thereof adhered to the active surface. The first rigid cover is made of a conducting material, an insulating material, or a transparent material.

[0015] In a preferred embodiment, the first terminal pads can be disposed around the circumference of the backside of the first chip area. The first terminal pads can also be disposed on the backside of the first chip area as an area array. Forming

the portions of the plurality of first connecting lines respectively in the plurality of through holes can be performed by electroplating. Besides, the first and second rigid covers are optionally structural connected with each other such that the process of sawing the wafer further comprises sawing the structural connection of the first and second rigid covers to separate the first and second rigid covers.

[0016] According to the chip package and the process thereof, a rigid cover is disposed on the active surface of the chip to protect the active surface of the chip and enhance the structural strength of the chip package. Further, if the material of the rigid cover is a thermal conductive material such as Cu or Al alloy, the heat-spread ability of the chip package can be enhanced. If the rigid cover is made of an electrical conductive material and electrically connected to the ground of the chip package, the electromagnetic interference (EMI) to the chip package can be reduced. It should be noted that the chip packaging process could form a plurality of the terminal pads on the backside of the chip so that the chip package can be connected to the PCB or substrate via these terminal pads.

[0017] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1A is a top view of the first chip package in accordance with the first embodiment of the present invention.

[0019] FIG. 1B is a cross-sectional view of the first chip package of FIG. 1A

along I-I' line.

[0020] FIG. 1C is a cross-sectional view of the first chip package of FIG. 1A connected to a printed circuit board.

[0021] FIG. 2A is a top view of the second chip package in accordance with the first embodiment of the present invention.

[0022] FIG. 2B is a cross-sectional view of the second chip package of FIG. 2A along II-II' line.

[0023] FIG. 2C is a cross-sectional view of the second chip package of FIG. 2A connected to a printed circuit board.

[0024] FIGs. 3A-3F show top views of the progression steps of the chip packaging process in accordance with the second embodiment of the present invention.

[0025] FIGs. 4A-4F show cross-sectional views of the chip packaging process of FIGs. 3A-3F along III-III' line.

[0026] FIG. 5 is a cross-sectional view of the chip package of FIG. 3F connected to a printed circuit board.

[0027] FIG. 6 is a cross-sectional view of another chip package connected to a printed circuit board in accordance with a second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] FIG. 1A is a top view of the first chip package in accordance with the first embodiment of the present invention. FIG. 1B is a cross-sectional view of the first chip package of FIG. 1A along I-I' line. Referring to FIGs. 1A and 1B, the chip package 100 includes a chip 110, a rigid cover 120, and an adhesive layer 130. The chip 110 is one of a plurality of unsawed chips of the wafer (not shown). The chip 110

has a rectangular shape having an active surface 112 and a plurality of bond pads 114. The bond pads 114 are disposed on the circumference of the active surface 112. The periphery of the rigid cover 120 is adhered to the active surface 112 via the adhesive layer 130. The bond pads 114 are disposed outside the periphery of the rigid cover 120.

[0029] FIG. 1C is a cross-sectional view of the first chip package of FIG. 1A connected to a printed circuit board. Referring to FIGs. 1A, 1B, and1C, a plurality of contacts 116 such as conductive bumps are disposed on the bond pads respectively. The heights of the contacts 116 relative to the active surface 112 are larger than the height of the rigid cover 120 relative to the active surface 112 so that the chip package 100 can be connected to the PCB 140 via the contacts 116. The PCB 140 has a plurality of contact pads 142. The bond pads 114 of the chip package 100 are electrically connected to the contact pads 142 of the PCB 140 via the contacts 116. Further, one can control the heights of the contacts 116 relative to the active surface 112 or the height of the rigid cover 120 relative to the active surface 112 to optionally make the rigid cover 120 contact or not contact the PCB 140. For thermal dissipation or electric characteristic consideration, the cover 120 can be structurally or electrically connected to the PCB 140. In FIGs. 1A-1C, the bond pads 114 are not limited to be disposed around the circumference of the active surface 112. The bond pads can also be disposed on one side or two sides (adjacent or opposite) of the active surface.

[0030] FIG. 2A is a top view of the second chip package in accordance with the first embodiment of the present invention. FIG. 2B is a cross-sectional view of the second chip package of FIG. 2A along II-II' line. Referring to FIGs. 2A and 2B, the chip 210 of the second chip package 200 has a plurality of bond pads 214 disposed as an

area array on the active surface 212. The active surface 212 of the chip 210 has a redistribution layer (not shown), which can rearrange the bond pads 214 around the circumference of the active surface 212 with an area array. Further, the rigid cover 220 is adhered to the active surface 212 via the adhesive layer 230. The rigid cover 220 has a plurality of openings 222 corresponding to the bond pads 214 and exposing the bond pads 214.

[0031] FIG. 2C is a cross-sectional view of the second chip package of FIG. 2A connected to a printed circuit board. A plurality of contacts 216 is disposed on the bond pads 214 respectively. The heights of the contacts 216 relative to the active surface 212 is larger than the height of the rigid cover 220 relative to the active surface 212 so that the chip package 200 can be connected to the PCB 240 via the contacts 116. The PCB 240 has a plurality of contact pads 242. The bond pads 214 of the chip package 200 are electrically connected to the contact pads 242 of the PCB 240 via the contacts 216.

[0032] In the above first and second chip packages, the rigid covers completely cover the wafers. A plurality of contacts such as conductive bumps, is disposed on the bond pads respectively. Then the wafer is sawed to obtain independent chip packages. It should be noted that although the contacts can be formed before sawing the wafer, one may also choose to form the contacts on the contact pads of the PCB. Then the chip package can be connected to the PCB via these contacts.

[0033] The second embodiment uses a plurality of connecting lines to extend the bond pads to the backside of the chip and to form the terminal pads on the backside of the chip.

[0034] FIGs. 3A-3F show top views of the progression steps of the chip

packaging process in accordance with the second embodiment of the present invention. FIGs. 4A-4F show the cross-sectional views of the chip packaging process of FIGs. 3A-3F along III-III' line. Referring to FIGs. 3A and 4A, a wafer 302 is provided. The wafer 302 has an active surface 312 and a backside 316 corresponding to the active surface 312. The wafer 302 has a first chip area 310a and a second chip area 310b adjacent to the first chip area 310a. The wafer 302 has a plurality of first and second bond pads 314a and 314b on the active surface 312 in the first and second chip areas 310a and 310b respectively.

[0035] Referring to FIGs. 3B and 4B, a plurality of through holes 318 are formed on the wafer 302. The through holes 318 are through the wafer 302 by laser drilling or mechanical drilling and connect the active surface 312 and the backside 316. The through holes 318 are arranged between the first chip area 310a and the second chip area 310b

[0036] Referring to FIGs. 3C and 4C, a plurality of first and second connecting lines 322a and 322b are formed on the wafer 302 by electroplating. Each of the first connecting lines 322a has a first end through one of the through holes 318 electrically connected to one of the first bond pads 314a. Each of the first connecting lines 322a has a second end extended to the backside 306 of the first chip area 310a to form one first terminal pad 324a on the backside 306 of the first chip area 310a. Each of the second connecting lines 322b has a first end through one of the through holes 318 electrically connected to one of the second bond pads 314b. Each of the second connecting lines 322b has a second end extended to the backside 306 of the second chip area 310b to form one second terminal pad 324b on the backside 306 of the second chip area 310b. It should be noted that because the first and second connecting lines 322a

and 322b are formed on the wafer 302 by electroplating, portions of the first connecting lines 322a in the through holes 318 may be connected to portions of the second connecting lines 322b in the through holes 318 respectively.

[0037] Referring to FIGs. 3D and 4D, a first rigid cover 320a and a second rigid cover 320b are disposed on the active surface 312 of the first chip area 310a and the active surface 312 of the second chip area 310b via the adhesive layers 330 respectively. For thermal dissipation or electric characteristic consideration, the first and second rigid covers 320a and 320b can be a conducting material, an insulating material, and a transparent material. Further, the chip packaging process can be a wafer level packaging process. Hence, the first and second rigid covers 320a and 320b can be a single structure. That is, the first and second rigid covers 320a and 320b can be structurally connected via a connecting bar 320c or other connecting structures. Therefore, only a single action is required to dispose the first and second rigid covers 320a and 320b on the active surface 312.

[0038] Referring to FIGs. 3E and 4E, the wafer 302 is sawed along an area between the first and second chip areas 310a and 310b by mechanical or laser sawing. The portions of the first connecting lines 322a in the through holes 318 and the portions of the second connecting lines 322b in the through holes 318 are also sawed. Hence, the lateral side of the chip 310 has a plurality of concave surfaces 318a (i.e., a half of the through holes 318). The portions of the first connecting lines 322a in the through holes 318 and the portions of the second connecting lines 322b in the through holes 318 are disposed on the concave surfaces 318a to electrically connect the bond pads 314 and the terminal pads 324. Further, when the first and second rigid covers 320a and 320b is a single structure, the connecting bars 320c will be sawed to separate the first and

second rigid covers 320a and 320b.

[0039] Referring to FIGs. 3F and 4F, the first chip area 310a and the second chip area 310b are separated from the wafer 302 by mechanical or laser sawing. Hence, the first chip area 310a and the first rigid cover 32a become a first chip package 300a, the second chip area 310b and the second rigid cover 320b become a second chip package 300b.

[0040] FIG. 5 is a cross-sectional view of the chip package of FIG. 3F connected to a printed circuit board. The chip package 300 includes a chip 310, a rigid cover 320, and an adhesive layer 330. The chip 300 has a rectangular shape and an active surface 312 and a plurality of bond pads 314. The bond pads 314 are disposed on the circumference of the active surface 312. A plurality of connecting lines 322 extend the bond pads 314 to the backside 316 of the chip 310 to form a plurality of the terminal pads 324. The terminal pads 324 can be connected to the contact pads 342 of the PCB 340 via a pre-solder, ACP or ACF (not shown).

[0041] FIG. 6 is the cross-sectional view of another chip package connected to a printed circuit board in accordance with the second embodiment of the present invention. Compared to FIG. 5, the chip 310 of the second chip package 300 has a plurality of terminal pads 324 disposed as an area array on backside 316 of the chip 310. These terminal pads 324 can be connected to the contact pads 342 of the PCB 340 via the contacts 350 such as conductive bumps.

[0042] The second embodiment uses a plurality of connecting lines to extend the bond pads to the backside of the chip and to form the terminal pads on the backside of the chip. Hence, when the chip is connected to the PCB, the active surface of the chip can be exposed. When the rigid cover is a transparent material, the chip package in the

second embodiment can be applied in optical-electronic devices such as CMOS image sensor (CIS) and solar cell, or bio-chip.

[0043] In brief, the chip package and the process thereof dispose a rigid cover on the active surface of the chip to protect the active surface of the chip and enhance the structural strength of the chip package. Further, if the material of the rigid cover is a thermally conductive material such as Cu or Al alloy, the heat-spread ability of the chip package can be enhanced. If the rigid cover is made of an electrical conductive material and electrically connected to the ground of the chip package, the electromagnetic interference (EMI) to the chip package can be reduced. If the rigid cover is a transparent material, the chip package can be applied in optic-electric or bio devices. In addition, the chip packaging process can form a plurality of the terminal pads on the backside of the chip so that the chip package can be connected to the PCB or substrate via these terminal pads.

[0044] The above description provides a full and complete description of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.